

1   Phase Conjugate Circuit

2

3   This invention relates generally to phase conjugate  
4   circuits and specifically, but not exclusively, to  
5   phase conjugate circuits containing phase locked  
6   loop circuits.

7

8   Phase conjugation of a particular signal is useful  
9   in numerous applications. One example is in retro-  
10   directive antenna arrays, where an incoming signal  
11   is automatically re-transmitted in the same  
12   direction as it was incident on the array by  
13   transmitting the phase conjugate of the incoming  
14   signal. Another example is in LINC (Linear  
15   Amplification using Non-Linear Components)  
16   amplifiers, where an amplitude modulated signal is  
17   firstly converted to a phase modulated signal and a  
18   phase conjugate modulated signal before being

1 amplified by non-linear amplifiers. The two  
2 amplified signals are then recombined to provide an  
3 amplified version of the original signal.

4  
5 In both these applications obtaining the phase  
6 conjugate of the incoming signal is an essential  
7 part of the electrical circuit.

8  
9 Phase conjugation circuitry, to some extent, has  
10 limited the commercialisation of both Retro-  
11 directive antenna arrays and LINC circuit  
12 architectures. For example, prior art phase  
13 conjugate circuits for retro-directive arrays use a  
14 heterodyning approach involving a signal mixer which  
15 relies on a local oscillator (LO) operating at twice  
16 the desired input RF (Radio Frequency) frequency. As  
17 the RF signal and the signal from the output IF  
18 (Intermediate Frequency) ports are the same, or very  
19 nearly the same, direct leakage from the RF signal  
20 to the IF ports causes significant problems. In  
21 addition the LO frequency must be twice the RF  
22 frequency so that the down-converted IF output  
23 signal is the phase conjugate of the RF input  
24 signal. This can be disadvantageous when the RF  
25 signal is required to be of very high frequency such  
26 as for anti-collision vehicular radars operating at  
27 77 GHz. In this case, the LO frequency would have to  
28 be 154GHz which would be difficult to construct  
29 using currently available technology.

30  
31 LINC amplifiers suffer from general circuit  
32 complexity in the phase conjugate sections.

1 Subsequently, LINC amplifiers have not been  
2 successfully operated at frequencies of greater than  
3 a few 10's of Megahertz mainly for this reason.

4  
5 Additional problems exist with the prior art  
6 associated with phase conjugation circuitry:  
7 prominent amongst these are the requirement for:

- 8 • sophisticated mixer balancing techniques required  
9 to prevent unwanted leakage signals corrupting  
10 the phase conjugation process. This leads to weak  
11 output signal levels since conventional mixer  
12 circuits are either passive (and therefore lossy)  
13 or limited to the few dB conversion gain that can  
14 be achieved with conventional active mixers; and  
15 • the need for a local oscillator signal operating  
16 at twice the RF signal (as mentioned above).

17  
18 Other applications for retrodirective (self  
19 tracking) array technology include simplex and  
20 duplex communication with low earth orbiting, non-  
21 geosynchronous satellites and as a low cost means  
22 for automatic beamforming as required for modern  
23 spatial division multiple access mobile phone  
24 wireless communication systems. Further examples are  
25 the use of a self-tracking array for automatic  
26 alignment of ground stations with high altitude  
27 communications platforms or in the creation of agile  
28 radar cross-section modification.

29

30 Phase locked loop circuits have been widely used  
31 since first being proposed in 1922. Since that time,  
32 PLL's have been used in instrumentation, space

1 telemetry and many other applications requiring a  
2 high degree of noise immunity and narrow bandwidth.

3

4 A standard phase lock loop (PLL) circuit comprises a  
5 phase detector, a low-pass filter, and an  
6 oscillator, usually a voltage-controlled oscillator  
7 (VCO). In the case where the oscillator is a VCO,  
8 the phase detector outputs a voltage proportional to  
9 the phase difference between a PLL input and a  
10 feedback signal from the output of the VCO. The low-  
11 pass filter acts as an integrator and provides a  
12 filtered voltage signal or an error signal which  
13 controls the VCO. When the error signal is zero, the  
14 VCO operates at a set frequency, known as the free  
15 running frequency. When the error signal is not  
16 zero, the phase of the PLL input and the feedback  
17 signal are no longer in balance and the VCO reacts  
18 to the error signal by modifying its output to track  
19 the PLL input.

20

21 It is an object of the present invention to obviate  
22 or mitigate the problems identified above in  
23 relation to phase conjugation circuits.

24

25 According to a first aspect of the present invention  
26 there is provided a circuit arrangement for deriving  
27 phase conjugation information from a main input  
28 signal of a given frequency comprising:

29       an input receiving a reference input signal;  
30       at least one phase locked loop circuit  
31       comprising an oscillator having a main output  
32       signal, an input receiving a PLL input signal, an

1 input receiving a feedback signal from the  
2 oscillator and at least one phase detecting means,  
3 wherein the phase detection means detects any phase  
4 difference between the PLL input signal and the  
5 feedback signal and provides a phase control signal  
6 to the oscillator.

7  
8 In one embodiment, the circuit arrangement further  
9 comprises a first heterodyne mixer having an input  
10 for receiving the main input signal and an input for  
11 receiving the main output signal, the first mixer  
12 providing the feedback signal and wherein the PLL  
13 input signal is the reference input signal.

14  
15 Preferably the feedback signal is the up-converted  
16 mixing product of the first heterodyne mixer.

17  
18 Preferably, the frequency of the reference input  
19 signal is scaled to match the frequency of the  
20 feedback signal.

21  
22 Further preferably, the feedback signal is scaled.

23  
24 Preferably, the phase detection means is a digital  
25 phase detector.

26  
27 In one form of the invention, the phase detection  
28 means also detects any phase difference between an  
29 input receiving the main output signal and an input  
30 receiving the reference signal thereby creating a  
31 further phase locked loop.

32

1 Preferably, the phase detection means comprises:  
2       a first phase detector which detects any phase  
3 difference between an input receiving the reference  
4 input signal and an input receiving the feedback  
5 signal;  
6       a second phase detector which detects any phase  
7 difference between an input receiving the reference  
8 input signal and an input receiving the main output  
9 signal;  
10       an integrator integrating the first phase  
11 detector output;  
12       an oscillator heterodyne mixer mixing the  
13 integrator output and the second phase detector  
14 output;  
15       wherein the oscillator mixer output is the  
16 phase detection means output providing a control  
17 signal for the oscillator.  
18  
19 In an alternative form of the invention, the phase  
20 detection means comprises:  
21       a first phase detection heterodyne mixer mixing  
22 an input receiving the reference input signal and an  
23 input receiving the feedback signal and having a  
24 first phase detection mixer output wherein the first  
25 mixer output is the down-converted mixing product of  
26 the first mixer;  
27       a second phase detection heterodyne mixer  
28 mixing an input receiving the reference input signal  
29 and an input receiving the first phase detection  
30 mixer output and having a second phase detection  
31 mixer output wherein the second phase detection  
32 mixer output is the down-converted mixing product of

1 the second phase detection mixer and the phase  
2 detection means output providing a control signal  
3 for the oscillator.

4  
5 In alternative form of the invention, a feedback  
6 heterodyne mixer mixes an input receiving the main  
7 output signal and an input receiving the reference  
8 input signal, the feedback signal is the down-  
9 converted mixing product of the feedback heterodyne  
10 mixer and the PLL input signal is the main input  
11 signal, the feedback signal being proportional to  
12 the main input signal.

13  
14 Preferably, the main input signal is scaled by a  
15 first divider, the main output signal is scaled by a  
16 second divider and the feedback signal scaled by a  
17 third divider, the first divider having a scaling  
18 value equal to the product of the second and third  
19 divider scaling values.

20  
21 Preferably, an input heterodyne mixer mixes the main  
22 input signal and the reference input signal, the PLL  
23 input signal is the down-converted mixing product of  
24 the input heterodyne mixer and the feedback signal  
25 is the main output signal, the main input signal and  
26 the main output signal having substantially equal  
27 frequencies.

28  
29 Preferably, a first divider scales the main input  
30 signal, a second divider scales the main output  
31 signal, the first divider having a scaling value  
32 equal to the second divider scaling value.

1

2 Preferably the oscillator is a voltage controlled  
3 oscillator (VCO).

4

5 According to a second aspect of the present  
6 invention there is provided a method of deriving  
7 phase conjugation information from an input signal,  
8 the method comprising detecting phase difference in  
9 a phase locked loop (PLL) circuit between an input  
10 receiving a feedback signal having a first frequency  
11 and an input receiving a PLL input signal of a  
12 second frequency which is proportional to the first  
13 frequency.

14

15 Embodiments of the present invention will now be  
16 described with reference to the accompanying  
17 drawings, in which;

18

19 Fig. 1 shows a schematic diagram of a frequency  
20 offset phase conjugating phase locked loop (PLL)  
21 circuit;

22

23 Fig. 2 shows a schematic diagram of a practical  
24 implementation of the phase conjugating PLL circuit  
25 of Fig. 1;

26

27 Fig. 3 shows a graphical representation of  
28 experimentally derived phase angle of signals in the  
29 phase conjugating PLL circuit of Fig. 2;

30

31 Fig. 4 shows a schematic diagram of an integrator  
32 based phase conjugating PLL circuit;



1

2 Fig. 5 shows a schematic diagram of a heterodyne  
3 mixer based phase conjugating PLL circuit.

4

5 Fig. 6 shows a schematic diagram of an alternative  
6 embodiment of a phase conjugating PLL circuit.

7

8 Fig. 7 shows a schematic diagram of a further  
9 alternative embodiment of a phase conjugating PLL  
10 circuit.

11

12 Referring now to Fig. 1, a frequency offset phase  
13 conjugating PLL circuit 100 has a main input signal  
14 102 ( $F_{in} + \phi$ ) and a reference input signal 104 ( $F_{REF}$ ). A  
15 reference divider 106 divides the reference input  
16 signal 104 and a main divider 108 divides a feedback  
17 signal 109 such that a phase detector 110 receives  
18 the divided reference input signal and the divided  
19 feedback signal at the same frequency. The phase  
20 detector outputs a phase control signal representing  
21 a phase difference between the reference input  
22 signal and the feedback signal 109. A low-pass loop  
23 filter 112 filters, or integrates, the phase control  
24 signal to provide a DC control signal. A voltage  
25 controlled oscillator (VCO) 114 receives the phase  
26 control signal and outputs a VCO signal 116 of a  
27 particular frequency ( $F_{VCO}$ ) and a phase angle ( $\phi$ )  
28 determined by the phase control signal. The VCO  
29 signal 116 is also a phase conjugate signal of the  
30 main input signal 102 as explained below. A  
31 heterodyne mixer 118 mixes the VCO signal 116 and  
32 the main input signal 102 to produce the feedback

1 signal 109 which in this case is filtered by a band  
2 pass filter 120 to allow selection of the up-  
3 converted mixing product of the mixer 118.

4

5 The frequency offset phase conjugating PLL circuit  
6 100 works in the following manner:

7

8 Up-converted Phase locked Loop without reference  
9 divider 106 and main divider 108

10

11 Output of mixer 118 :  $F_{IN} + \phi + F_{VCO} + \varphi$

12 Reference Input 104 :  $F_{REF} = F_{IN} + F_{VCO}$

13 At position C :  $F_{IN} + F_{VCO} = F_{IN} + \phi + F_{VCO} + \varphi$

14 :  $F_{IN} + F_{VCO} - F_{IN} - \phi + F_{VCO} - \varphi = 0$

15 :  $-\phi - \varphi = 0$

16 :  $\varphi = -\phi$

17 VCO signal 116 :  $F_{VCO} + \varphi = F_{VCO} - \phi$

18

19 Therefore, if  $F_{VCO} = F_{IN}$ , the VCO signal 116 is the  
20 phase conjugate of the main input signal 102.

21 If  $F_{VCO} \neq F_{IN}$  then the VCO signal 116 is the offset  
22 phase conjugate of the main input signal 102.

23

24 The reference divider 106 and the main divider 108  
25 allow the possibility of reducing the required  
26 frequency of the reference input signal 104. The  
27 phase detector 110 is intended to detect any  
28 difference in phase between the feedback signal 109  
29 and the reference input signal 104.

30

31 For example:

1         $F_{IN} = 1000\text{MHz}$   
2         $F_{VCO} = 990\text{MHz}$   
3         $F_{REF} = 10\text{MHz}$   
4        Input to Main divider (up-converted) = 1990MHz  
5        Output from Main divider =  $1990/9950 = 0.2\text{MHz}$   
6        Input to Reference divider = 10MHz  
7        Output from Reference divider =  $10/50 = 0.2\text{MHz}$

8  
9        Using this arrangement, the reference input signal  
10       104 at a much smaller frequency than the main input  
11       signal 102 is required.

12  
13       Referring now to Fig. 2, a phase conjugating PLL  
14       circuit 200, that is an experimental implementation  
15       of the frequency offset phase conjugating PLL  
16       circuit of Fig. 1, is shown. A main input signal 202  
17       and a reference input signal 204 are generated from  
18       a first signal synthesiser 206. A phase shifter 203  
19       is introduced to the main input signal 202 so that  
20       the main input signal 202 has a different phase  
21       angle than that of the reference input signal 204. A  
22       first power splitter 205 splits the main input  
23       signal 202 so that an oscilloscope 230 can visually  
24       display the signal 202 without any losses. A  
25       Philips® UMA1021M PLL chip contains a reference  
26       input divider 210, a main input divider 212 and a  
27       phase detector 214. In this example, the reference  
28       input divider 210 divides the reference input signal  
29       204 which is then inputted to the phase detector  
30       214. The main input divider 212 divides a feedback  
31       signal 216 which is then also inputted to the phase  
32       detector 214. The phase detector produces a phase

1 control signal 218 which represents the phase  
2 difference between the reference input signal 204  
3 and the feedback signal 216. A loop filter 220  
4 integrates the phase control signal 218. A unity  
5 gain non-inverting summing amplifier 222 ensures the  
6 phase control signal 218 is isolated from the phase  
7 detector 214 and also allows the phase control  
8 signal 218 to be offset as necessary. A Voltage  
9 Controlled Oscillator (VCO) 224 has an output signal  
10 226 at a predetermined frequency. The VCO can vary  
11 the phase of the output signal 226 dependent on the  
12 phase control signal 218. A second power splitter  
13 228 allows the output signal 226 to be displayed on  
14 the oscilloscope 230 without any losses within the  
15 circuit 200. The output signal 226, when the circuit  
16 200 is phase locked, is now a phase conjugate signal  
17 of the main input signal 202. A heterodyne mixer 232  
18 mixes the output signal 226 and the main input  
19 signal 202 to produce the feedback signal 216. A  
20 band-pass filter 234 filters the feedback signal 216  
21 such that only the up-converted mixing product from  
22 the mixer 232 remains. A third power splitter 236  
23 allows the feedback signal to be analysed by a  
24 microwave transition analyser (MTA) 238 as well as  
25 being connected to the main divider 212 without any  
26 losses to the circuit 200. A second signal  
27 synthesiser 240 provides a comparison signal 242 to  
28 the oscilloscope 230 and the MTA 238 as required.  
29 The main input signal 202 and the comparison signal  
30 242 are phase locked to the reference input signal.  
31

1 In use, the first signal synthesiser 206 synthesised  
2 the main input signal 202 at a frequency of 1.05GHz  
3 and the reference input signal 204 at 0.01GHz. The  
4 phase shifter 203 introduces a different phase angle  
5 to the main input signal 202 than that of the  
6 reference input signal 204. The main input signal  
7 202 is then viewed on the oscilloscope 230 via the  
8 first power splitter 205. The main output signal 226  
9 is generated by the VCO 224 at a frequency of  
10 0.94GHz and is also viewed on the oscilloscope 230  
11 via the second power splitter 228. The mixer 232  
12 mixes the main input signal 202 and the main output  
13 signal 226. The band-pass filter 234 ensures that  
14 only the up-converted mixing product forms the  
15 feedback signal 216 at a frequency of 1.99GHz. The  
16 feedback signal 216 is viewed on the MTA 238 via the  
17 third power splitter 236. The main input divider 212  
18 divides the feedback signal 216 by 9950 producing a  
19 signal of 200KHz. The reference divider divide the  
20 reference input signal 204 by 50 to also produce a  
21 signal of 200KHz. The phase detector 214 then  
22 detects the phase difference between the divided  
23 feedback signal 216 and the divided reference input  
24 signal 204 to produce the phase control signal 218  
25 which ultimately controls the VCO's 224 phase angle.  
26 The second signal synthesiser 240 is used to  
27 generate different signals as required for  
28 comparison purposes. Therefore, the comparison  
29 signal 242 is set to 0.94GHz for comparison with the  
30 main output signal. As the comparison signal 242 is  
31 phase locked to the reference input signal 202, the  
32 main output signal 226 should be a phase conjugate

1 of the comparison signal and therefore the phase  
2 difference can be measured to confirm this. To  
3 measure the actual phase of the main input signal  
4 202 after it had been phase shifted by the phase  
5 shifter 203, the second synthesised source 240 is  
6 set to produce a comparison signal 242 of 1.05GHz.  
7 To further validate that phase conjugation was  
8 operating correctly it was important that the  
9 feedback signal 216 had constant phase. The second  
10 synthesised source 240 is set to produce a  
11 comparison signal 242 of 1.99GHz and the MTA 238  
12 used to analyse the feedback signal 216.

13  
14 Referring now to Fig. 3 a graphical representation  
15 of a non-conjugated phase angle 302 (representing  
16 the main input signal 202 of Fig.2) is matched  
17 substantially equally and oppositely to a conjugated  
18 angle 304 (representing the output signal 226 of  
19 Fig. 2). A conjugation error 306 is also shown  
20 representing the error in phase angle in the  
21 conjugated angle 304. It can be clearly seen from  
22 Fig. 3 that the conjugated angle 304 has only a  
23 small conjugation error 306 at any time and that the  
24 practical implementation circuit 202 effectively  
25 produces a frequency offset phase conjugated output.

26  
27 Referring now to Fig. 4, an alternative embodiment  
28 of a phase conjugation PLL circuit 400 is shown. The  
29 circuit 400 has a PLL 402 and a loop 404. A  
30 reference signal 406 supplies a reference signal to  
31 both the PLL 402 and the loop 404. The PLL 402 has a  
32 first phase detector 408 which compares a first

1 feedback signal 410 with the reference signal 406. A  
2 summer 412 receives a first phase error signal 414  
3 and a second phase error signal 416 to produce a  
4 composite phase control signal 418. A VCO 419  
5 produces an output signal 420 with a phase dependent  
6 on the phase control signal 418. A second heterodyne  
7 mixer 422 mixes a main input signal 424 with the  
8 output signal 420 to produce a second feedback  
9 signal 426. A second phase detector 428 compares the  
10 phase of the second feedback signal and the  
11 reference signal 406 producing a second phase  
12 detector output 430. An integrator 432 integrates  
13 the second phase detector output 430 producing the  
14 second phase error signal 416.

15

16 In use, the circuit 400 has a fast acting PLL 402  
17 that establishes a frequency lock. The loop 404 is  
18 relatively slower because of the integrator's 432  
19 transfer characteristics. The loop 404 then forces  
20 the output signal 420 to the conjugate phase of the  
21 main input signal 424.

22

23 Referring now to Fig. 5, an alternative embodiment  
24 of a phase conjugation PLL circuit 500 is shown. A  
25 first heterodyne mixer 502 mixes a main input signal  
26 504 and an output signal 506 to produce a feedback  
27 signal 508. The feedback signal 508 is the up-  
28 converted mixing product of the first heterodyne  
29 mixer 502. A second heterodyne mixer 510 mixes a  
30 reference signal 512 with the feedback signal 508  
31 producing an intermediate signal 514. The  
32 intermediate signal 514 is the down-converted mixing

1 product of the second heterodyne mixer 510. A third  
 2 heterodyne mixer 516 mixes the intermediate signal  
 3 514 with the reference signal 512 producing a phase  
 4 control signal 518. The phase control signal 518 is  
 5 the down-converted mixing product of the third  
 6 heterodyne mixer 516. A VCO 520 produces an output  
 7 signal 506 with a phase dependent on the phase  
 8 control signal 518.

9  
 10 The operation of the circuit 500 is explained below.

11  
 12 Assuming that the circuit 500 is phase locked and  
 13 the main input signal ( $RF_{IN}$ ) 504, the output signal  
 14 ( $RF_{OUT}$ ) 506 and the reference signal ( $RF_{REF}$ ) 512 are  
 15 all the same frequency  $\omega$ .

16 The feedback signal 508 is  $RF_F$ , the intermediate  
 17 signal 514 is  $RF_I$  and the phase control signal 518  
 18 is  $RF_C$ .

19

$$20 \quad RF_{REF} = \omega + \theta_{REF}$$

$$21 \quad RF_{IN} = \omega + \theta_{IN}$$

$$22 \quad RF_{OUT} = \omega + \theta_{OUT}$$

$$23 \quad RF_F = 2\omega + \theta_{OUT} + \theta_{IN}$$

$$24 \quad RF_I = \omega + \theta_{OUT} + \theta_{IN} - \theta_{REF}$$

$$25 \quad RF_C = \theta_{OUT} + \theta_{IN} - \theta_{REF} - \theta_{REF} = c$$

$$26 \quad \theta_{OUT} = c + 2\theta_{REF} - \theta_{IN}$$

27

28 In the equation above it is shown that the output  
 29 signal phase is conjugated to the main input signal  
 30 phase ( $\theta_{OUT} = -\theta_{IN}$ ). The term  $c + 2\theta_{REF}$  represents a  
 31 static phase error introduced by the reference input



1 signal's 512 oscillator. The  $2\theta_{REF}$  term may be  
2 removed by filtering. The term  $c$  represents the  
3 control voltage for the VCO 520 and therefore will  
4 always be present except where the output frequency  
5 is equal to the free-running frequency of the VCO  
6 520. The term  $c$  will change as the circuit 500  
7 tracks changes in the main input signal 504  
8 frequency.

9  
10 For retrodirective antenna arrays this does not pose  
11 a problem as relative phase states are important,  
12 not absolute phase states. For LINC type amplifier  
13 applications any phase error caused by the term  $c$   
14 can be accounted for by a prior calibration process  
15 across the expected frequency operating range of the  
16 circuit.

17  
18 The circuit 500 can instantaneously phase conjugate  
19 as the circuit is made up of heterodyne mixers and  
20 does not include integrators or phase detectors  
21 which have a finite time determined by the loop  
22 dynamics in order to establish a phase lock. As the  
23 heterodyne mixers act as the phase detectors, the  
24 circuit 500 can operate directly at the microwave  
25 and millimetre wave frequencies without the need for  
26 dividers or digital phase detection circuitry.

27  
28 Referring now to Fig. 6, an alternative embodiment  
29 of a phase conjugation PLL circuit 600 is shown. A  
30 reference input signal ( $\omega_c + \psi$ ) 602 and a main output  
31 signal ( $\omega + \phi_1$ ) 604 are supplied to a mixer 606. In  
32 this example, an output divider 608 divides the main

1 output signal 604 by  $N_1$ . A first low-pass filter 610  
2 receives and filters the output of the mixer 606 to  
3 extract the down-converted mixing product and  
4 produce a feedback signal 612. A feedback divider  
5 614 divides the feedback signal 612 by  $N_2$ . A phase  
6 detector 616 receives the output from the feedback  
7 divider 614.

8

9 An input divider 620 receives a main input signal  
10  $(\omega_1 + \theta_i)$  618 and divides by  $N_3$ . The main input signal  
11 is then inputted to the phase detector 616.

12

13 The phase detector 616 outputs a phase control  
14 signal 621 representing a phase difference between  
15 the feedback signal 612 and the main input signal  
16 618. A second low-pass filter 622 filters, or  
17 integrates, the phase control signal 621 to provide  
18 a DC control signal 623. A VCO 624 outputs the main  
19 output signal 604 according to the DC control signal  
20 623.

21

22 The operation of the circuit 600 is explained below.

23

24 At point A the main output signal 604 is divided by  
25 the output divider 608:

26

27

$$\frac{\omega}{N_1} + \frac{\phi_i}{N_1}$$

28 At point B the reference signal 602 is mixed by the  
29 mixer 606 with the main output signal 604 after  
30 division by the output divider 608 and filtered by  
31 the first low-pass filter 610 to extract the down-  
32 converted mixing product:

1

2

$$\omega_c + \psi - \frac{\omega}{N_1} - \frac{\phi_i}{N_1}$$

3

4

At point C the down converted mixing product of the mixer 606 is divided by the feedback divider 614:

5

6

$$\frac{\omega_c}{N_2} + \frac{\psi}{N_2} - \frac{\omega}{N_2 N_1} - \frac{\phi_i}{N_2 N_1}$$

7

8

9

At point D the main input signal 618 has been divided by the input divider 620:

10

11

$$\frac{\omega_1}{N_3} + \frac{\theta_i}{N_3}$$

12

13

At point E the phase detector 616 compares the signal at point C and the signal at point D:

14

15

16

$$\frac{\omega_c}{N_2} + \frac{\psi}{N_2} - \frac{\omega}{N_2 N_1} - \frac{\phi_i}{N_2 N_1} - \frac{\omega_1}{N_3} - \frac{\theta_i}{N_3}$$

17

18

When the circuit 600 has phase lock, the output of the phase detector 616 is zero:

19

20

$$\frac{\omega_c}{N_2} + \frac{\psi}{N_2} - \frac{\omega}{N_2 N_1} - \frac{\phi_i}{N_2 N_1} - \frac{\omega_1}{N_3} - \frac{\theta_i}{N_3} = 0$$

21

22

If  $\frac{\omega_1}{N_3} = \frac{\omega_c}{N_2} - \frac{\omega}{N_2 N_1}$  and  $\psi = 0$ , as it is the reference signal phase, then:

23

24

25

$$-\frac{\phi_i}{N_2 N_1} = \frac{\theta_i}{N_3}$$

26

27

Provided  $N_3 = N_2 N_1$  then  $\theta_i = -\phi_i$  and phase conjugation occurs.

28

29

30

31

32

Referring now to Fig. 7, an alternative embodiment of a phase conjugation PLL circuit 700 is shown. A main input signal ( $\omega_1 + \theta_i$ ) 702 is divided by an input divider 704 to provide an input for a mixer 706

1 along with a reference signal ( $\Delta f + \psi$ ) 708. A first  
 2 low-pass filter 710 enables extraction of the down-  
 3 converted mixing product of the mixer 706. A phase  
 4 detector 712 receives the down-converted mixing  
 5 product of the mixer 706 and a feedback signal 714  
 6 and outputs a phase control signal 715. A second  
 7 low-pass filter 716 filters the phase control signal  
 8 715 to generate a DC control signal 718. An  
 9 oscillator 720 receives the DC control signal 720  
 10 and generates a main output signal ( $\omega + \phi_i$ ) 722,  
 11 which, in this case, is also the feedback signal  
 12 714. A feedback divider 724 divides the feedback  
 13 signal 714 before the feedback signal 714 is  
 14 inputted to the phase detector 712.

15

16 The operation of the circuit 700 is explained below.  
 17

18 At point A the main input signal 702 has been  
 19 divided by the input divider 704:

$$20 \quad \frac{\omega_1}{N_1} + \frac{\theta_1}{N_1}$$

22 At point B the divided main input signal and the  
 23 reference signal 708 have been mixed with the down-  
 24 converted mixing product being extracted:

25

$$26 \quad \Delta f + \psi - \frac{\omega}{N_1} - \frac{\theta_1}{N_1}$$

27

28 At point C the main output signal 722 has been  
 29 divided by the feedback divider 724:

30

$$31 \quad \frac{\omega}{N_2} + \frac{\phi_i}{N_2}$$

32

1

2

3 At point D the phase detector 712 compares the  
4 signal at point B and the signal at point C:

5

6

$$\Delta f + \psi - \frac{\omega_1}{N_1} - \frac{\theta_i}{N_1} - \frac{\omega}{N_2} - \frac{\varphi_i}{N_2}$$

7

8 When the circuit 700 has phase lock, the output of  
9 the phase detector 712 is zero:

10

11

$$\Delta f + \psi - \frac{\omega_1}{N_1} - \frac{\theta_i}{N_1} - \frac{\omega}{N_2} - \frac{\varphi_i}{N_2} = 0$$

12 If  $N_1 = N_2 = N$ , then  $\omega = \omega_1$ , and  $\psi = 0$ , as it is the  
13 reference signal phase, then:

14

$$\Delta f N - 2\omega - \theta_i - \varphi_i = 0$$

15 or,

16

$$\theta_i = -\varphi_i + (\Delta f N - 2\omega)$$

17 So, if  $\Delta f N = 2\omega$ , then  $\theta_i = -\varphi_i$  and phase conjugation  
18 occurs.

19

20 Improvements and modifications may be incorporated  
21 without departing from the scope of the present  
22 invention.

23